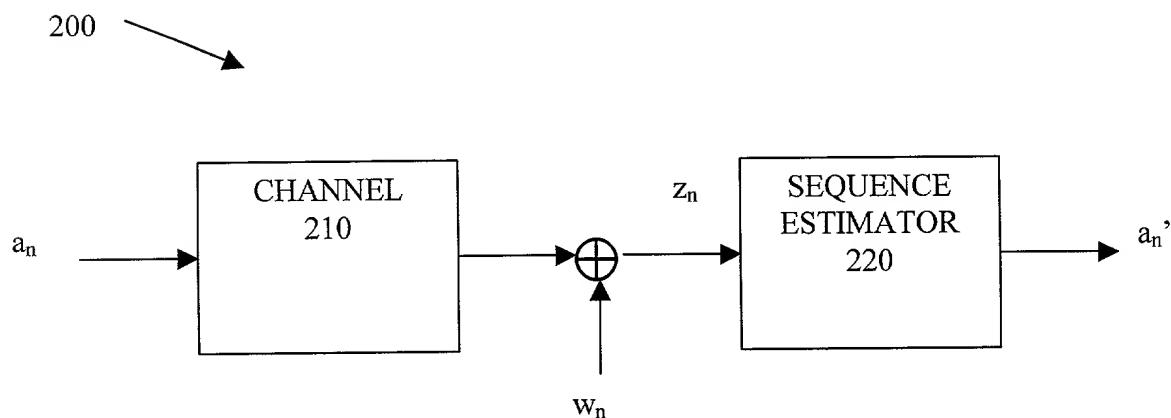
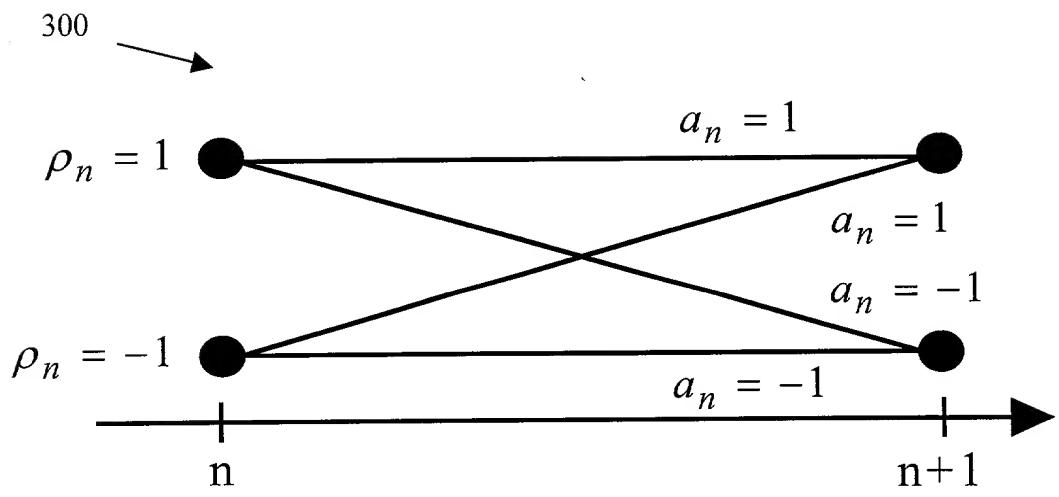


**FIG. 1**

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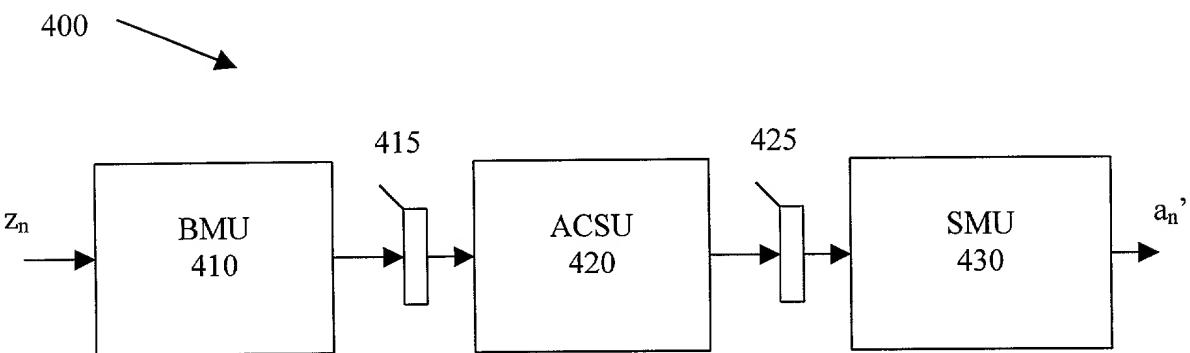


**FIG. 2**

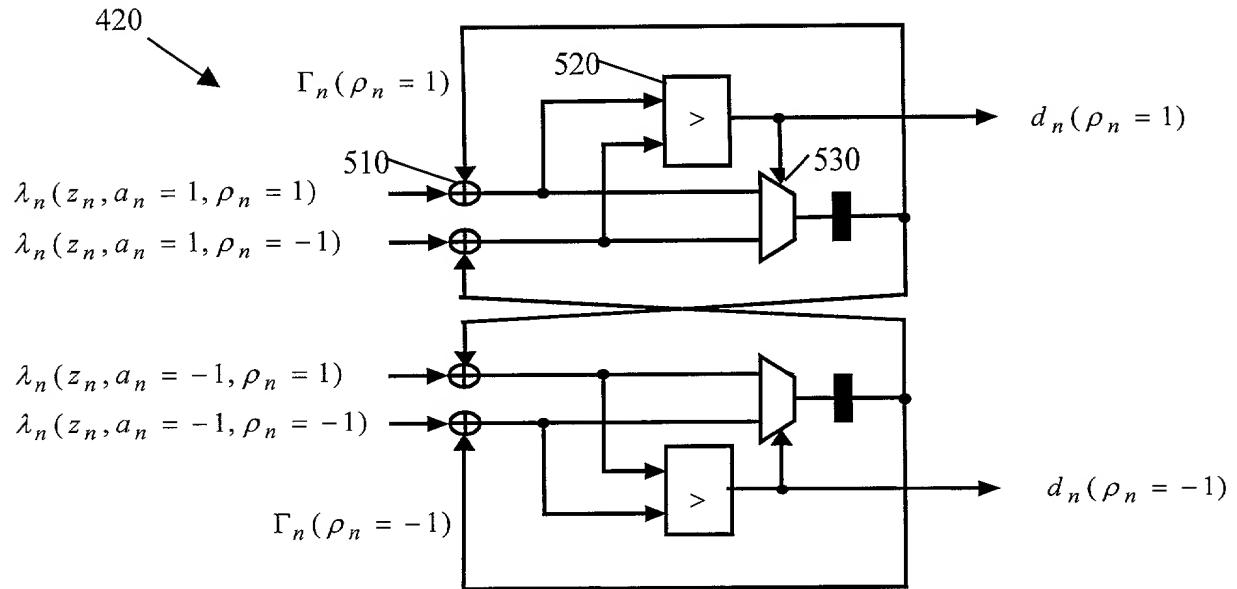


**FIG. 3**

A schematic diagram of a three-stage signal processing system. The stages are represented by rectangular boxes: BMU 410, ACSU 420, and SMU 430. An input signal  $z_n$  enters the BMU 410 stage. The output of BMU 410 is labeled 415. This signal then enters the ACSU 420 stage, whose output is labeled 425. Finally, the signal enters the SMU 430 stage, whose output is labeled  $a_n'$ . Arrows indicate the flow of signals between the stages.



**FIG. 4**

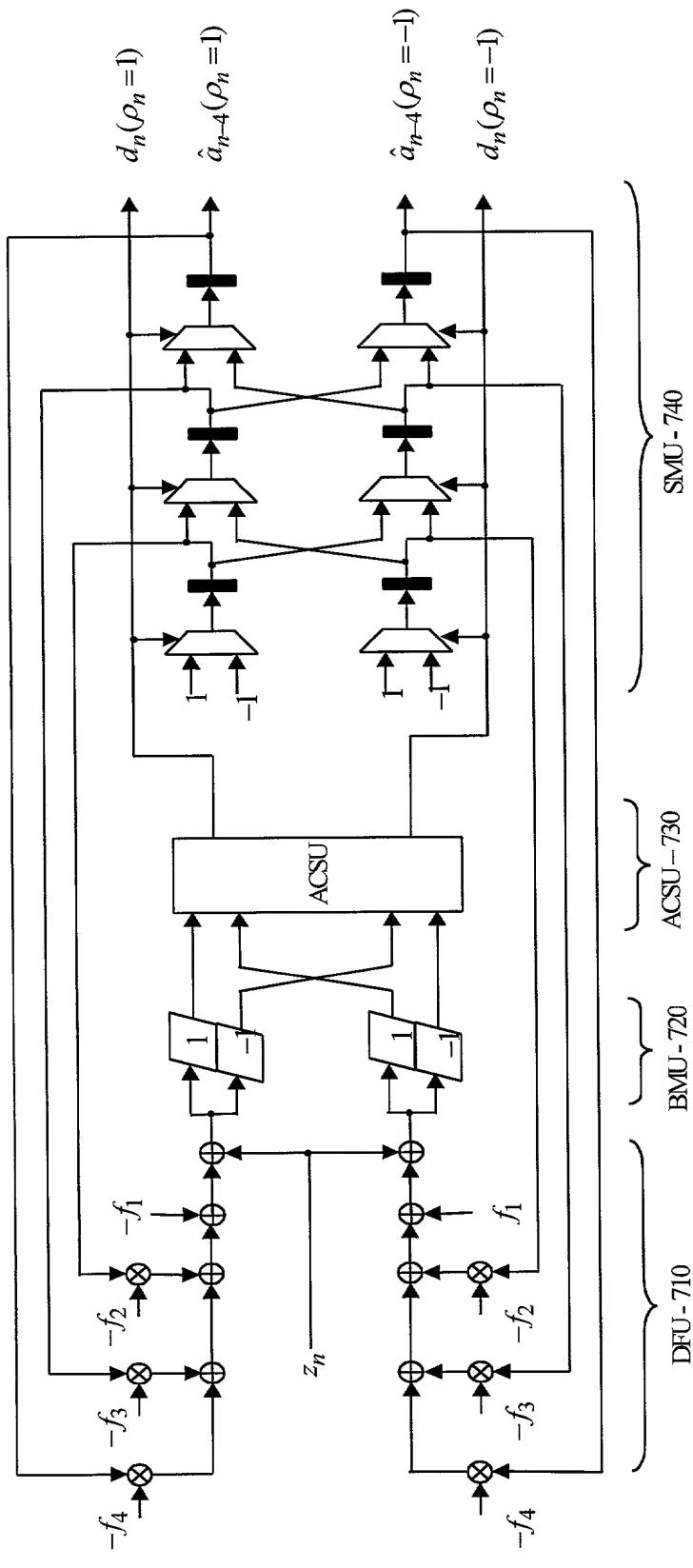


**FIG. 5**

Complexity and Critical Path Analysis Table -- 600

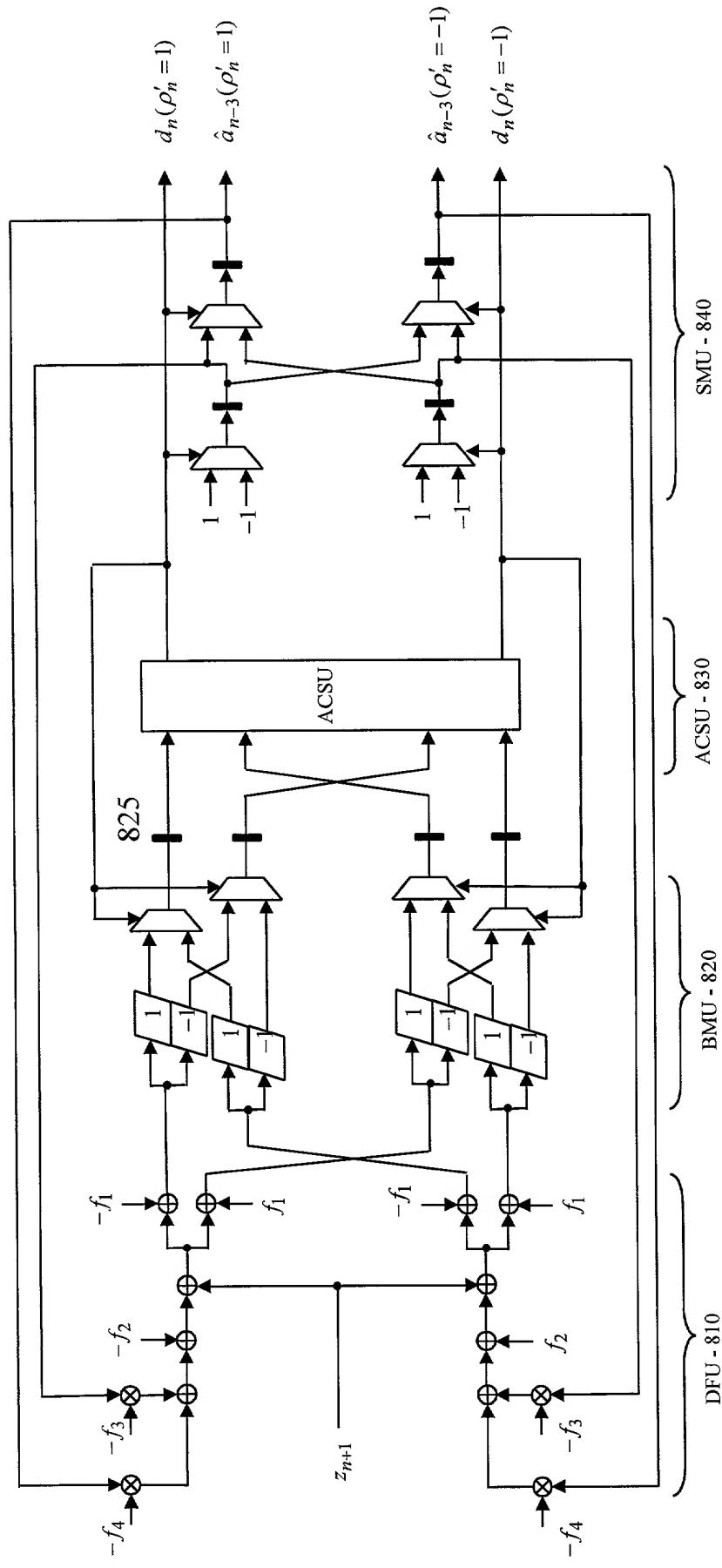
	MLSE <u>620</u>	RSSE <u>630</u>
<b>Complexity</b>		
No. of states:	$2^L$	$2^K$
No. of BMs	$2^{L+1}$	$2^{K+1}$
ADDS in DFU:	—	$S \times L$
<b>Critical path</b>	2 ADDs 2-to-1 MUX	$L-K+3$ ADDs 2-to-1 MUX LUT SHIFT

**FIG. 6**

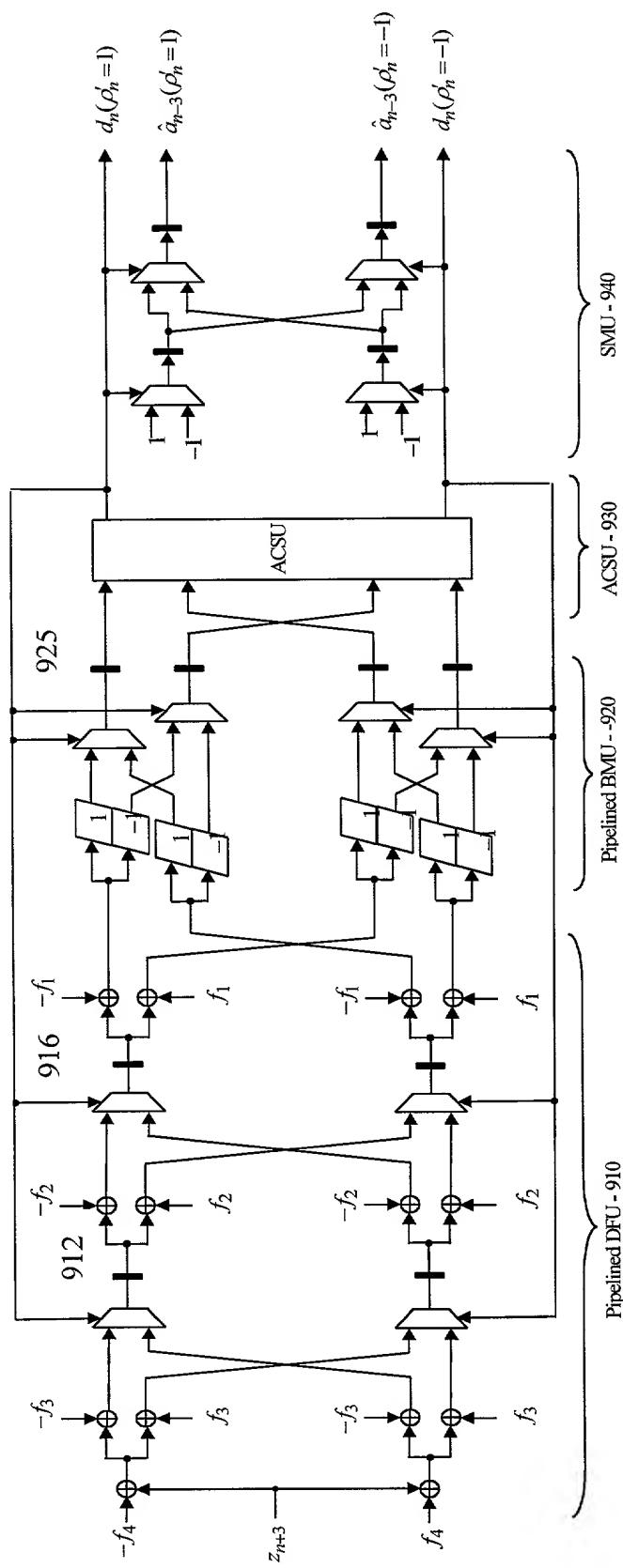
**FIG. 7A**

$$x \rightarrow c \rightarrow y \equiv y = (x - c)^2$$

**FIG. 7B**



**FIG. 8**

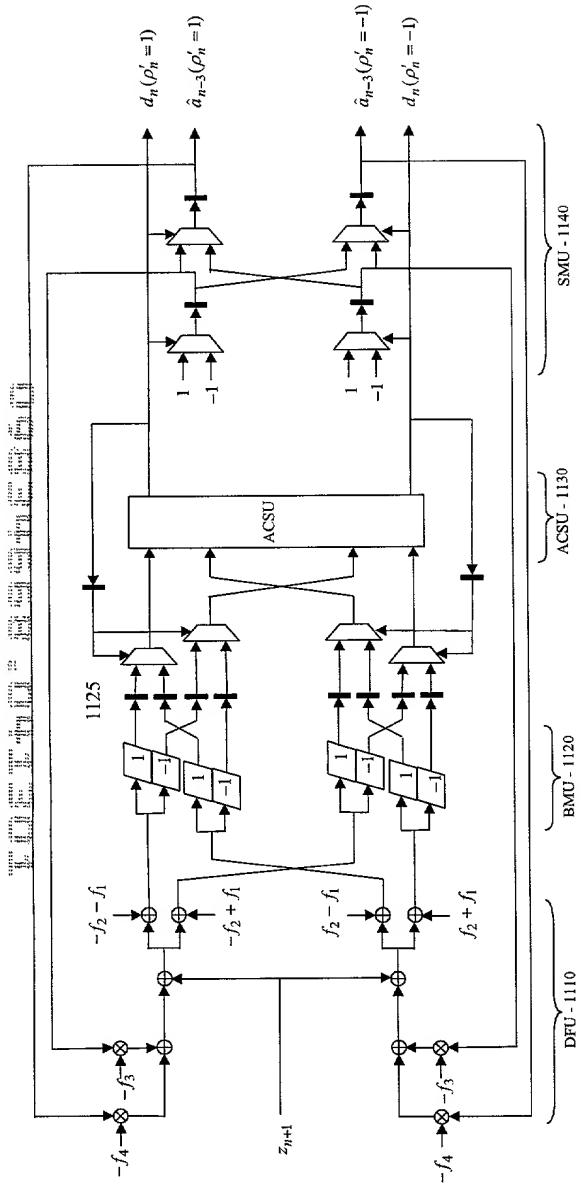


**FIG. 9**

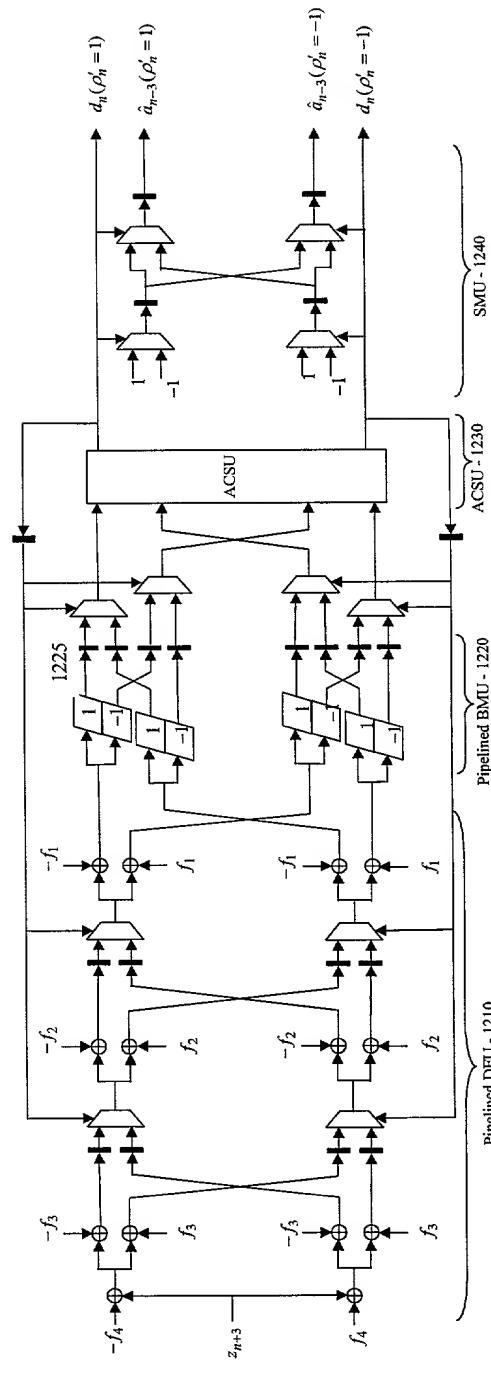
Complexity and Critical Path Analysis Table of Pipelined RSSE - 1000

	Pipelined RSSE
<b>Complexity</b>	
No. of BMs:	$2^{K+2}$
ADDs in DFU:	$S \times (L-M+2M) = S \times (L+M)$
<b>Critical path (<math>M=L-K</math>)</b>	2 ADDs 2-to-1 MUX

## FIG. 10



**FIG. 11**



**FIG. 12**

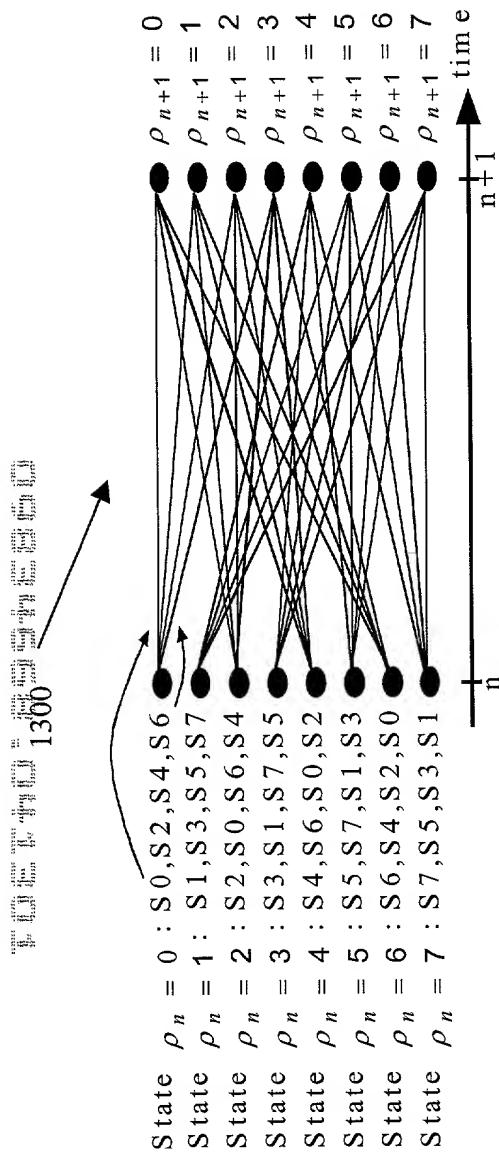


FIG. 13

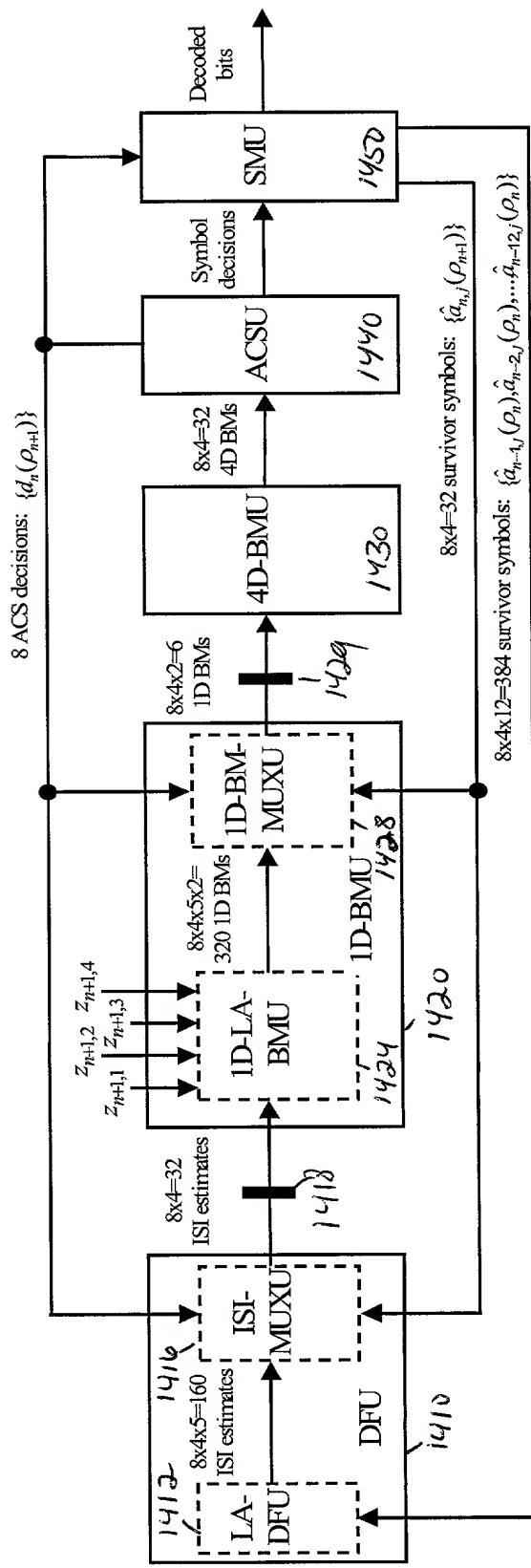


FIG. 14

1412

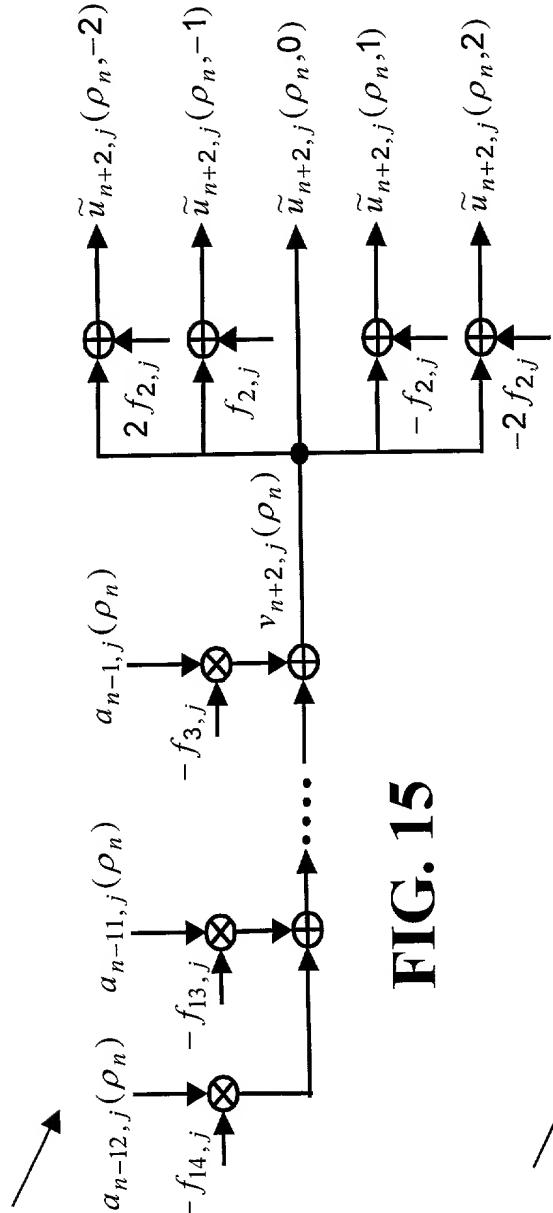


FIG. 15

1416

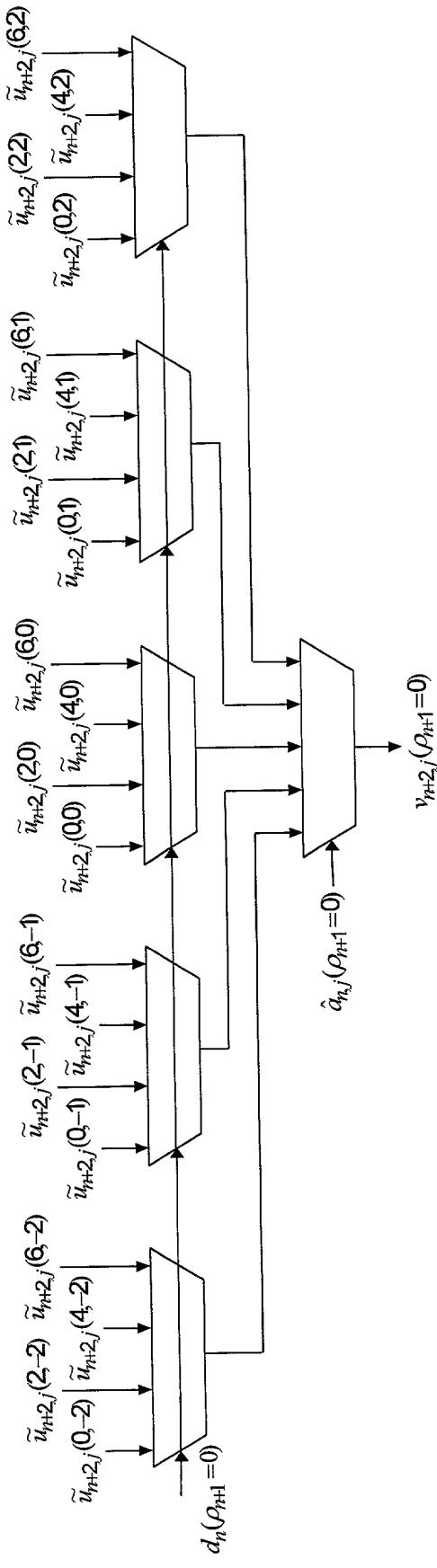


FIG. 16

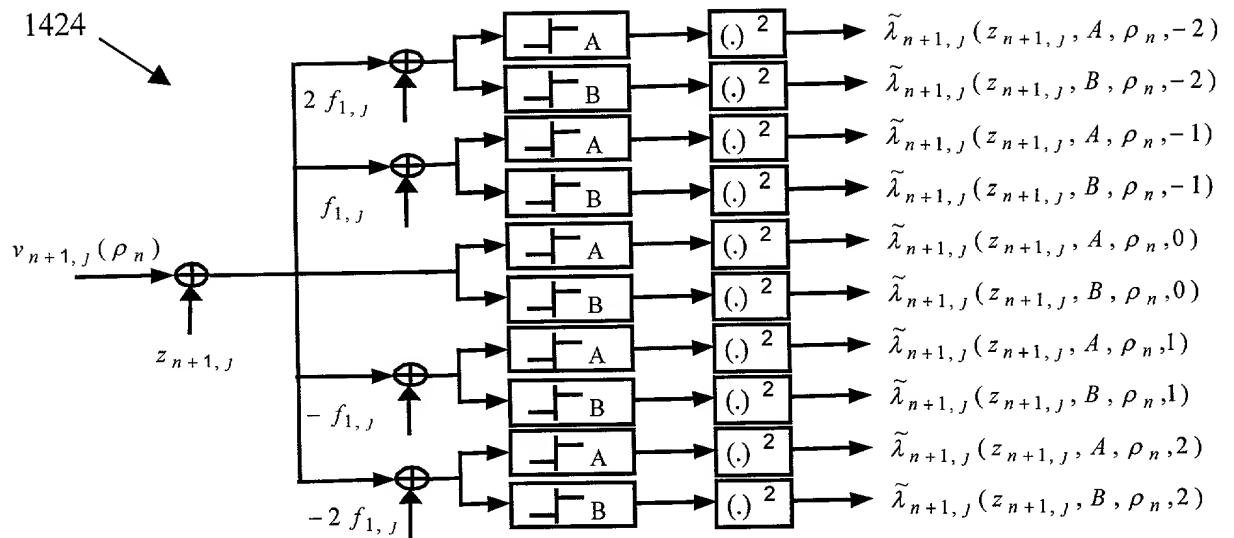


FIG. 17

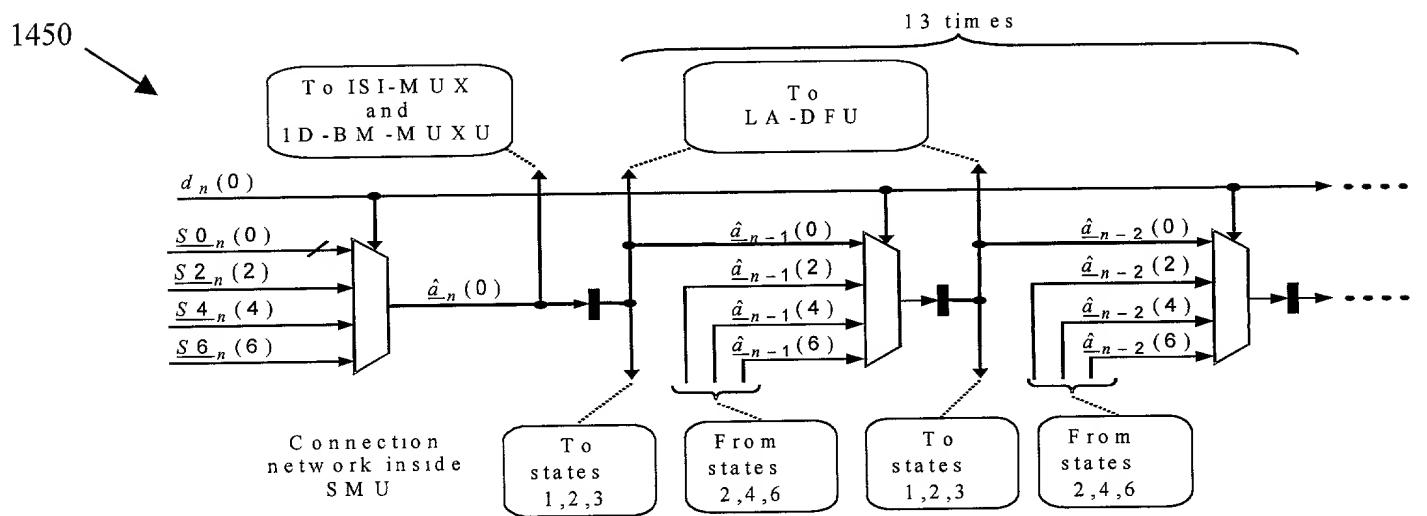


FIG. 18